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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/575,625	04/13/2006	Hiromitsu Sakai	Q78084	4644

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EXAMINER
HU, SHOUXIANG

ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/575,625	SAKAI ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-14 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-14 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata (Shibata et al., US 2002/0155682; of record).

Shibata discloses a Group-III nitride semiconductor element (Figs. 1-4; also see [0065] through [0071]), comprising a substrate (such as sapphire single crystal) with a first nitride semiconductor layer (AlN) provided thereon (similar to what is included in layer 1 shown in Figs. 1-3); a second nitride semiconductor layer composed of $Al_{x1}Ga_{1-x1}N$ (similar to layer 2 in Figs. 1-3; such as: $Al_{0.1}Ga_{0.9}N$, with x1 = 0.1; island-shaped) provided on the first nitride semiconductor layer; and, a third nitride semiconductor layer composed of $Al_{x2}Ga_{1-x2}N$ (similar to layer 3A in Figs. 2 and 3; such as: $Al_{0.95}Ga_{0.05}N$, with x2 = 0.95) provided on the second nitride semiconductor layer.

Furthermore, the first nitride semiconductor layer (AlN) in Shibata is naturally a substantially single crystal, since it is epitaxially grown on the single crystal substrate at a substantially high temperature of 1200^0 C (see [0066]), and/or, since it is grown with a material set and/or process condition that are both substantially same as that in the instant invention (see page 9, lines 16-22, in the instant specification).

Shibata does not expressly disclose that the thickness of the first nitride semiconductor layer (AlN) can be of a thickness between 0.005 to 0.5 um, and/or that the Al composition ratio x1 for the second nitride semiconductor layer can be a value that is larger than 0 but no larger than 0.05 or 0.02. However, Shibata does expressly disclose that the thickness of the first nitride semiconductor layer (AlN) can be 1um, and that the Al composition ratio x1 for the second nitride semiconductor layer can be 0.1, which are respectively within the range with the thickness and the range for the Al composition ratio x1 of disclosed in the instant invention; and they are respectively substantially close to the relevant upper limits of what are recited in the present claims for such thickness and composition ratio.

Furthermore, it is noted that it is art known that the AlN layer (i.e., the first nitride semiconductor layer) functions as a buffer layer and such as buffer layer can commonly have a thickness that is well within such recited thickness range (as readily evidenced in the prior art such as Mitamura of US 6,475,923, which has a 0.05um-thick AlN buffer layer; see col. 9, lines 39-41). And, Shibata further expressly discloses that lower Al composition ratio in the second nitride semiconductor layer, as compared with that in the first nitride semiconductor layer, can desirably reduce dislocation density (see [0047] and [0048]).

And, it is further noted that the thickness and the composition ratio are both art-recognized result-oriented important parameters, subject to routine experimentation and optimization.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the Group-III nitride semiconductor element of Shibata with the thickness of the AlN layer therein being a value (such as 0.05 um or 0.5 um) that is within a range such as between 0.01 and 0.5 um, and/or with the Al-composition ratio x1 in the second nitride semiconductor layer being reduced to a value (such as 0.05 or 0.02 or 0.01) that is substantially within a range such as between 0.001 and 0.05, so that a semiconductor element with optimized performance and/or with reduced dislocation density and/or with optimized process conditions would be obtained, as it has been held that:

"[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 3, it is further noted that the second nitride semiconductor layer in Shibata is formed of the islands (2-1 through 2-4) arranged separately from one another; and, the crystals in theses islands inherently have different heights, as they are self-formed (i.e., without the help of any masks) through a MOCVD method, in a manner substantially same as that in the instant invention.

Regarding claims 4 and 16, it is further noted that the second nitride semiconductor layer in Shibata naturally has a region having a lower Al content at a position near the interface between the second and third nitride semiconductor layers but closer to the substrate, and a higher Al content at a position also near the interface between second and third nitride semiconductor layers but further/farther from the

substrate, given that the third semiconductor layer in Shibata is formed on the second one at a temperature that is substantially high, which naturally causes net Al diffusions (more or less, but definite exist) from the third nitride semiconductor layer to the second one, as the Al concentration in the third one is higher than that in the second one. And/or, the second nitride semiconductor layer in the above optimized semiconductor element would naturally have a region having a lower Al content at a position closer to the substrate and a higher Al content at a position further/farther from the substrate, since it would have a material composition and/or process condition that are substantially same as that of the instant invention.

Regarding claims 7-9, it is further noted that, although Shibata does not expressly discloses that the second nitride semiconductor layer can have a thickness of about 1 to 300 nm, such thickness is an art-recognized result-oriented parameter of importance, subject to routine experimentation and optimization. Therefore, it would also have been obvious to one of ordinary skill in the art at the time the invention was made to the make the device/element of Shibata with the second nitride semiconductor layer having a thickness that is within the recited range, so that a nitride-semiconductor device/element with optimized performance and/or process conditions would be obtained, as again it has been held that:

"[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 10, the second nitride semiconductor layer in Shibata is undoped.

Regarding claims 11 and 12, the Group-III nitride semiconductor element of Shibata is for the use in a Group III nitride semiconductor light-emitting device (see Fig. 4; a diode), further comprising a fourth nitride semiconductor layer (see layers 13-17) provided on said third nitride semiconductor layer of said semiconductor element, said fourth nitride semiconductor layer including an n-type layer (13 and/or 14), a light-emitting layer (15), and a p-type layer (16 and/or 17), which are successively formed atop said third nitride semiconductor layer in this order; a negative electrode (18) provided on said n-type layer; and a positive electrode provided on said p-type layer (19).

Regarding claim 13, it is further noted that it is well known in the art a Group-III nitride semiconductor element such as the one of Shibata can be readily and desirably used to form a laser with desired laser performance.

Response to Arguments

3. Applicant's arguments filed on 02/12/2009 have been fully considered but they are not persuasive. And, responses to them have been fully incorporated into the claim rejections set forth above in this office action.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference A is cited as being related to a substrate structure having an AlN buffer layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Friday, 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shouxiang Hu/
Primary Examiner, Art Unit 2811